

REMARKS

The Final Office Action mailed on June 25, 2002, has been received and reviewed. Claims 31-35 and 37-45 are currently pending in the application. Claims 31-35 and 37-45 stand rejected. Claims 31, 33, and 40 have been amended. Reconsideration of the application is respectfully requested.

35 U.S.C. § 112 Claim Rejections

Claims 37-41, 44, and 45 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

It is respectfully submitted that, contrary to the Examiner's indication that Applicant's FIGS. 7-10 show the HSG layer as being removed, the presence of HSG layer 122 is clearly shown in FIG. 8. Further, while the originally filed specification stipulates the removal of mask layer 124 prior to dielectric deposition, nowhere does the specification indicate the removal of the remaining HSG layer 122 (see Specification, page 8, lines 19-26).

It is, therefore, respectfully submitted that the originally filed specification of the above-referenced application supports all of the elements that are recited in claim 37-41 and 44-45 and, thus, the rejections under 35 U.S.C. § 112 are invalid.

Rejections Under 35 U.S.C. § 102

Kenney

Claims 35, 42, and 43 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,254,503 to Kenney (hereinafter "Kenney"). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kenney teaches the formation of sublithographic relief images to increase the surface area of semiconductor structures. The formation of the relief structure of region 14 can be the deposition of polysilicon. Col. 3 lines 51-65. Kenney does not expressly or inherently describe a contiguous layer, but rather illustrates region or surface 14 as discrete islands of hemispherical-grain polysilicon. See FIG. 1. Further, the hemispheres of region 14 are clearly separated by mask layer 16. See FIG. 2. After trenches are etched into the substrate 10, the regions of hemispherical-grain polysilicon contact no common surface. Even the bottom surfaces of the remaining hemispherical-grain polysilicon of region 14 contact only separate portions of region 12, divided by the trenches extending to region 10. See FIG. 4.

Claim 35 recites an intermediate semiconductor capacitor structure comprising a storage poly structure *with recesses formed therein*, and a *contiguous hemispherical-grain polysilicon layer* over the storage poly structure.

Kenney does not disclose a structure that includes a poly structure with recesses and a contiguous hemispherical-grain polysilicon layer. Rather, the hemispherical-grain polysilicon sections disclosed in Kenney are spaced apart, sharing no common boundary.

Therefore, Kenney does not disclose each and every element of claim 35. Accordingly, it is respectfully submitted that claim 35 is not anticipated by Kenney.

Claim 42 recites an intermediate semiconductor capacitor structure comprising a storage poly structure and a *substantially confluent hemispherical-grain polysilicon layer* over the storage poly structure. A generally accepted definition of “confluent” is flowing together: meeting or coming together: combining to form one. *See, e.g.* Webster’s Third New International Dictionary (Merriam Webster 1986).

Kinney does not disclose confluent regions of hemispherical-grain polysilicon. Rather than coming together, the hemispherical-grain polysilicon used in the Kinney method, when produced, is separated (See FIG. 1) and is further separated after the etching process (See FIG. 4).

Therefore, Kenney does not disclose each and every element of claim 42. Accordingly, it is respectfully submitted that claim 42 is not anticipated by Kenney.

Claim 43 recites an intermediate semiconductor capacitor structure comprising a storage poly structure including recesses, portions of a hemispherical-grain polysilicon layer over the storage poly structure, and a mask *spaced apart from storage poly structure by the hemispherical-grain polysilicon layer*.

Kenney does not disclose a mask spaced apart from a storage poly structure by a hemispherical-grain polysilicon layer. Rather than being spaced apart from the semiconductor substrate 10, the masking material 16 fills the recesses in the surface 14, contacting region 12 which may be of the same material of the substrate. See FIG. 2-4, Col 3 lines 39-42.

Therefore, Kenney does not disclose each and every element of claim 43. Accordingly, it is respectfully submitted that claim 43 is not anticipated by Kenney.

Rejections Under 35 U.S.C. § 103(a)

Ahn

Claims 31 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,358,888 to Ahn et al. (hereinafter "Ahn").

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Ahn teaches a method for manufacturing a capacitor. A polysilicon layer having hemispherical grains is formed on a substrate and used as an etch-mask. After a first etching, the hemispherical grain layer is eliminated during a second etching. Col. 8 lines 37-39.

Claim 31, as proposed to be amended herein, recites a semiconductor capacitor storage poly that includes downwardly extending recesses and a plurality of contiguous mesas including *contiguous top surfaces* and forming a maze-like structure. Rather than teaching a capacitor structure with elements have “contiguous” top surfaces and forming a “maze-like” structure, Ahn et al. describes individual islands of the capacitor structure that are laterally isolated from one another (see col. 6, lines 31-64). The *top surfaces* of the islands are clearly non-contiguous, sharing no common boundaries (see FIGs. 6 and 16). For this reason, it is respectfully submitted that Ahn et al. does not teach or suggest all of the limitations of claim 31.

Regarding obviousness, the Examiner presents no argument for a motivation to add these missing limitations, and there is nothing in the reference or from the knowledge generally available in the prior art which would lead one of ordinary skill to make the modification. Accordingly, Applicants respectfully submit claim 31 is allowable over Ahn et al. under 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a), and request the rejection be withdrawn.

Claim 32 is allowable, among other reasons, as depending from claim 31, which is allowable.

Ahn in View of Kenney

Claims 33, 34, and 38-41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ahn in view of Kenney.

The teachings of Ahn and Kenney have been summarized herein.

Claim 33, as proposed to be amended herein, recites a semiconductor capacitor storage poly that includes downwardly extending recesses and a plurality of contiguous mesas including *contiguous top surfaces* and forming a maze-like structure. Rather than teaching a capacitor structure with elements have “contiguous” top surfaces and forming a “maze-like” structure, Ahn et al. describes individual islands of the capacitor structure that are laterally isolated from one another (see col. 6, lines 31-64). The *top surfaces* of the islands are clearly non-contiguous, sharing no common boundaries (see FIGs. 6 and 16).

Further, neither Kenney nor Ahn, taken alone or in combination teach a semiconductor capacitor storage poly including hemispherical-grain polysilicon on the top surfaces of a plurality

of contiguous webs. As noted in the above-referenced Office Action, Ahn et al. fail to teach a HSG polysilicon on top surfaces (see page 4). Ahn et al. states “The HSG layer 80 is eliminated together with the conductive layer ...” (see col. 8, lines 29-47 and col 10, lines 42-49). Kenney states “Following the transfer of the masked pattern into the substrate, the mask forming layers can be removed and the substrate further processed as necessary” (see col. 4, lines 38-40 and Fig. 6). This plural “layers” indicates both the masking layer 16 and the HSG layer are removed. For these reasons, it is respectfully submitted that neither Ahn et al. nor Kenney teach or suggest all of the limitations of claim 33.

Claim 34 is allowable, among other reasons, as depending from claim 33, which is allowable.

Claim 38 recites a semiconductor memory cell structure having “regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure ... and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses”.

Neither Kennedy nor Ahn, taken alone or in combination teach a semiconductor memory cell structure including hemispherical-grain polysilicon on the top surfaces of a storage poly structure, coated by a dielectric layer. The HSG layer of both Kennedy and Ahn is removed before the addition of dielectric material, as noted herein. Therefor neither Ahn et al. nor Kenney teach or suggest all of the limitations of the rejected claims.

Claims 39 through 41 are each allowable, among other reasons, as depending from claim 38, which should be allowed.

Claim 40 is additionally allowable because claim 40 recites “said storage poly structure comprises a web-like structure comprising a plurality of *contiguous top surfaces*” (emphasis added). Ahn et al. and Kenney, on the other hand, describe individual islands that are laterally isolated from one another (see Ahn et al. at col. 6, lines 31-64 and FIGs. 6 and 16) and isolated columns on a storage poly structure (see Kenney at FIGs. 1 and 4).

Kenney

Claims 37-39, 41, 44, and 45 stand rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Kenney (U.S. Patent No. 5,254,503). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants respectfully submit the 35 U.S.C. § 103(a) obviousness rejections are improper because a *prima facie* case of obviousness has not been made.

Applicants respectfully submit Kenney fails to describe or teach or suggest all of the limitations of the rejected claims. Claim 37 recites an intermediate semiconductor memory cell structure having “low elevation regions of a hemispherical-grain polysilicon layer on said storage poly structure ... and dielectric material at least lining the recesses.” Claim 38 recites a semiconductor memory cell structure having “regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure ... and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses”. Claim 44 recites an intermediate semiconductor capacitor structure having “a hemispherical-grain polysilicon layer on at least portions of the storage poly structure ... and dielectric material lining at least said recesses.” Claim 45 recites an intermediate semiconductor memory cell structure having “a hemispherical-grain polysilicon layer on at least portions of the storage poly structure ... and dielectric material lining at least said recesses.”

Kenney, on the other hand, states “Following the transfer of the masked pattern into the substrate, the mask forming layers can be removed and the substrate further processed as necessary” (see col. 4, lines 38-40 and Fig. 6). As discussed above, this indicates the HSG is removed before the addition of dielectric material. For this reason, it is submitted that Kenney does not teach or suggest all of the limitations of claims 37, 38, 44 and 45.

Regarding obviousness, the Examiner presents no argument for a motivation to add the missing limitation, and there is nothing in the reference or from the knowledge generally available in the prior art which would lead one of ordinary skill to make the modification.

Accordingly, Applicants respectfully submits claims 37, 38, 44 and 45 are allowable over Kenney under 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a), and request the rejections be withdrawn.

Claims 39 and 41 are allowable, among other reasons, as depending from claim 38, which is allowable.

ENTRY OF AMENDMENTS

The proposed amendments to claims 31, 33, and 40 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, as the proposed amendments merely recite the previously recited subject matter more clearly, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 31 through 35 and 37 through 45 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,



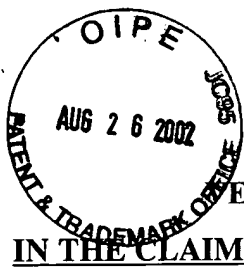
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Date: August 26, 2002

Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE
IN THE CLAIMS:

31. (Three times amended) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses; and
a plurality of contiguous mesas comprising a plurality of contiguous top surfaces forming a
maze-like structure.

33. (Three times amended) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses;
a plurality of contiguous webs comprising a plurality of contiguous top surfaces forming a maze-
like structure; and
hemispherical-grain polysilicon on at least some of said plurality of contiguous top surfaces [of at
least some of said plurality of contiguous webs].

40. (Twice amended) The semiconductor memory cell structure of claim 38, wherein
said storage poly structure comprises a web-like structure comprising a plurality of contiguous
top surfaces.